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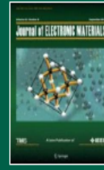

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Abstract

Silicon based technology encounters scaling parameters that prohibit the advancement of transistor technology. Graphene nanoribbons (GNR) and carbon nanotubes (CNT) are often considered the predominating devices to replace silicon technology. Carbon nanotube field effect transistors (CNTFETs) are considered the most promising devices because of their most interesting properties such as high current carrying ability (~1010 A/cm^2), excellent carrier mobility, scalability, high reliability for elevated temperature operation, and negligible leakage current. In this paper, a comparative analysis of CNTFET and graphene nanoribbon field effect transistors (GNRFET) is presented. The results of simulations are presented, and comparisons of devices are done based on different parameters listed as I_{ON}/I_{OFF} current ratio, trans-conductance, and inverse subthreshold slope using NanoTCAD ViDES. After simulation, it is shown that CNTFET offers better results for I_{ON}/I_{OFF} on the order of 10^6, subthreshold swing (SS) as 74.4 mV/dec, and

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Parameterized Comparison of Nanotransistors Based on CNT and GNR Materials: Effect of Variation in Gate Oxide Thickness and Dielectric Constant

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Silicon based technology encounters scaling parameters that prohibit the advancement of transistor technology. Graphene nanoribbons (GNR) and carbon nanotubes (CNT) are often considered the predominating devices to replace silicon technology. Carbon nanotube field effect transistors (CNTFETs) are considered the most promising devices because of their most interesting properties such as high current carrying ability ($\sim$ 1010 A/cm^2), excellent carrier mobility, scalability, high reliability for elevated temperature operation, and negligible leakage current. In this paper, a comparative analysis of CNTFET and graphene nanoribbon field effect transistors (GNRFET) is presented. The results of simulations are presented, and comparisons of devices are done based on different parameters listed as I_{ON}/I_{OFF} current ratio, trans-conductance, and inverse subthreshold slope using NanoTCAD ViDES. After simulation, it is shown that CNTFET offers better results for I_{ON}/I_{OFF} on the order of 10^6, subthreshold swing (SS) as 74.4 mV/dec, and transconductance as 7.6 μS. Further the effect of oxide thickness and dielectric constant has been studied for both FET devices. At the end, it is concluded that CNTFET offers better simulation result than that of GNRFET.

Key words: Carbon nanotube, carbon nanotube field effect transistor, graphene nanoribbon field effect transistor, NanoTCAD ViDES

INTRODUCTION

According to Moore's Law, devices are further shrinking as the technology scaling factors go beyond the sub-nanometer regime. Hence, researchers are switching to nanoscale semiconductor devices because complementary metal oxide semiconductor (CMOS) transistors scale down to their fundamental physical limit.[1] The carbon nano-tube (CNT) is a modern alteration of carbon, discovered by S. Lijima of NEC Corp in Tokyo, while studying electron microscope images. A CNT is composed of strong covalent C–C bonds with a perfect crystalline structure. Carbon has one innovative property among all elements, in that it forms a long chain of its own atoms, known as catenation. Depending on the number of tubes used as a channel, it is either a single-wall nanotube (SWNT) or multi-wall nanotube (MWNT), as shown in Fig. 1a and b, respectively. CNTs are composed of 1-D graphene sheets that attain a cylindrical tube shape after rotating around an axis. CNTs can be formed of different diameters and microscopic dimensions, depending on the conditions in which the graphene sheet is rolled into cylinders. CNTs have an important feature in that they can behave as either metallic or semiconducting. The innovation here is the mechanism of transport of electrons from the source to the drain.[2]

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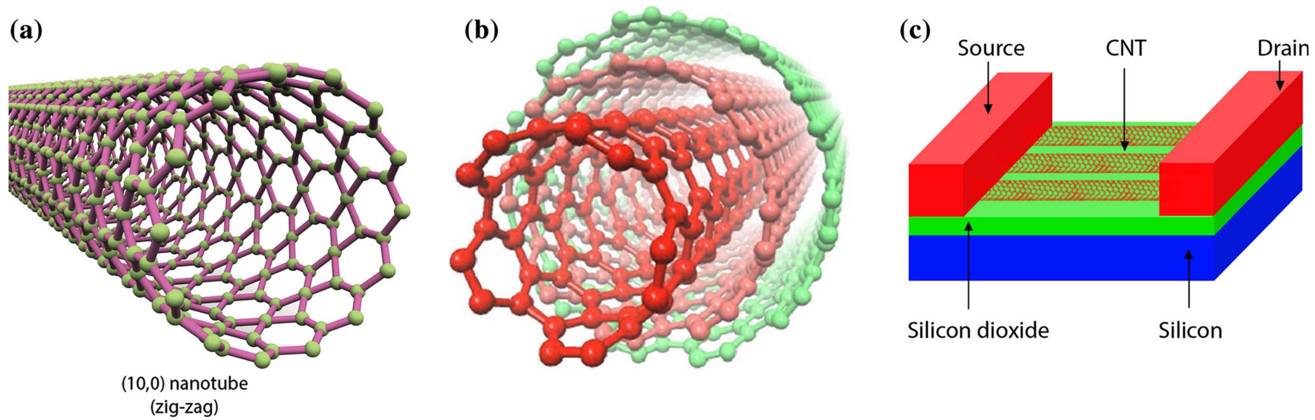

Fig. 1. Structure model of a CNT: (a) SWNT, (b) MWCNT, (c) Descriptive diagram of CNTFET.

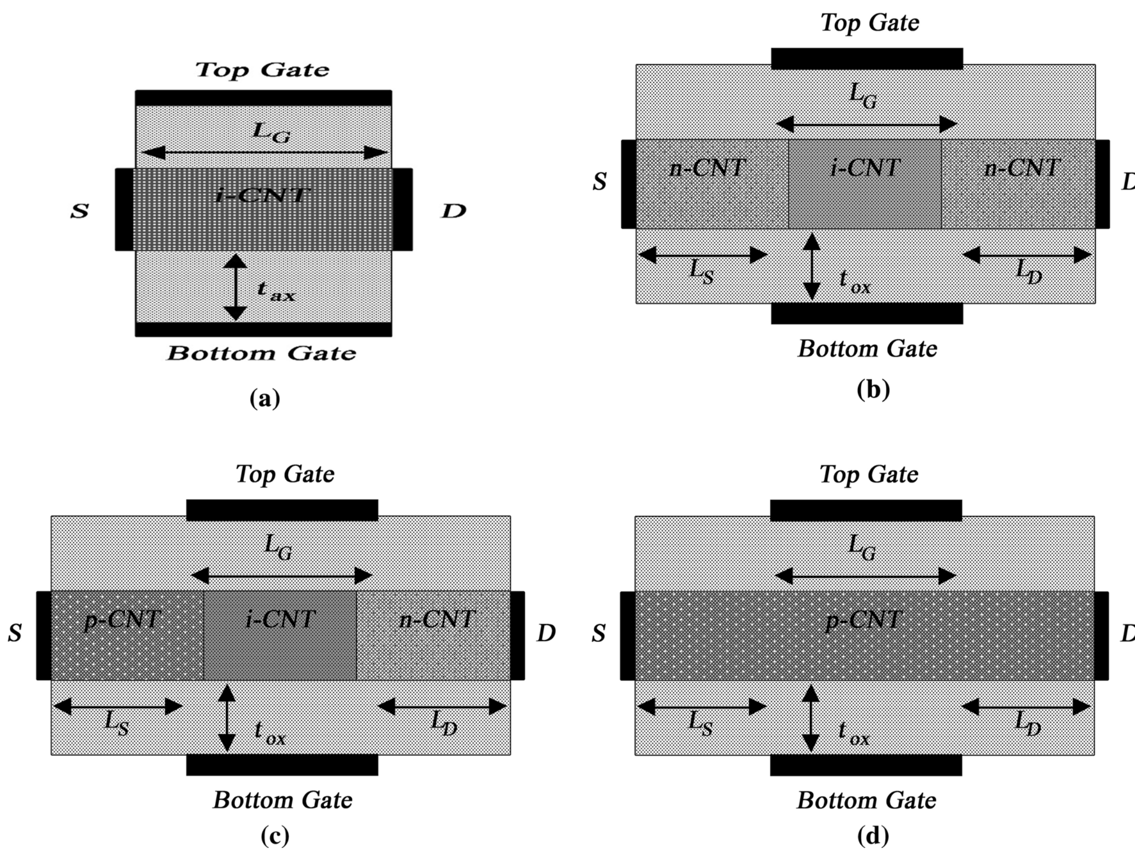

Fig. 2. Types of CNTFET: (a) SB-CNTFET, (b) C-CNTFET, (c) T-CNTFET, (d) Partially gated CNTFET.

A carbon nanotube field effect transistor (CNTFET) does not suffer those issues that challenged the CMOS technology.[3] The CMOS design framework can be reused because device formation of CNTFETs is very much similar to metal oxide semiconductor field effect transistors (MOSFET). CNTs act as the channel transmission, which acts as the transport mechanism and is also considered the backbone of CNTFETs.[4,5]

Graphene is defined as the formation of a one-atom-thick sheet of carbon atoms, which results in a hexagonal structure. It is a monolayer ribbon of graphene, which is induced through a particular channel transport direction, in which its narrow channel width reveals its interesting electronic properties theoretically and experimentally. Graphene is a zero-gap, two-dimensional material; hence, due to the absence of channel formation, it is not suited for switching functionality. So, the energy gap can be induced by using a lithography process of the sides by making narrow graphene strips called graphene nanoribbons. A non-equilibrium Green's function (NEGF) is a definite quantum transport technique used to study devices in the

nanoscale regime. Graphene nano-ribbons (GNR) present many fascinating properties and the expectation of ultrahigh carrier mobilities exceeding those of the conventional semiconductors. This has encouraged much work on the development of graphene-based field effect transistors. Graphene MOSFETs show complete switch-off and large on–off ratios with GNR channels that have been validated for future logic circuitry.[6] Though the mentioned drain current models agreed well with experiments and included many fitting parameters, they are inconvenient for applications. Graphene-based devices have received much consideration as a rising technology.

CNFET DEVICE STRUCTURE

The carbon nanotube (CNT) is an outstanding substitute for conventional silicon technology towards forthcoming nano-electronics because of its individual promising electrical properties. The excellent mechanical and novel electrical properties of CNTs such as high tensile durability, long mean free path, good electrical conductivity, high thermal potential, light weight and hardness act as the driving force for their applications in chip interconnects.[7,8] CNTFETs are of various types known as Schottky Barrier-CNTFET (SB-CNTFET), partially gated (PG-CNTFET), conventional-CNTFET (C-CNTFET), and tunnel-CNTFET (T-CNTFET). A descriptive diagram of the CNTFET is shown in Fig. 1c.

Figure 2a shows an SB-CNTFET, in which channel forms of intrinsic CNT are established as a straight metal contact at both source and drain sides. Because of the intrinsic nature of channel, ambipolar characteristics are realized. To suppress the ambipolar effects, various methodologies must be used. The value of the current for electron injection is greater in relation to hole injection because it depends less on drain voltage. The physical dimensions of a Schottky Barrier play an integral role, as electrons and holes concentrate from which an electron can jump or tunnel from the metal surface to the CNT channel. The failure of SB-CNTFET is that the inverse subthreshold slope always attains greater value for simulated data than theoretical data value as 60 mV/dec.[9] CNTs have a large mean free path, so there is no scattering of charge carriers at the channel length of 100 nm even in the nanoscale range. The diameter (D_{CNT}) of a nanotube and the chiral angle (θ) are measured by its chiral vector coordinates as described by Eqs. 1 and 2, respectively.[10]

$$D_{\mathrm{CNT}} = \sqrt{3}\frac{a}{\pi}\sqrt{m^2+n^2+mn} \tag{1}$$

$$\cos\theta = \frac{\frac{(n+m)}{2}}{\sqrt{n^2+m^2+mn}} \tag{2}$$

where a is the carbon–carbon bond distance and is given as 0.246 nm. Current in CNTFETs can be easily changed either by changing the diameter of the tube or by making use of more than one tube as a channel. If $n = m$ then the carbon nanotubes are metallic, when $n - m = 3i$ with small gap they are semi-metallic and when $\mathrm{n} - \mathrm{m} \neq 3i$, they are semiconductors (i is an integer). Equation 3 states that the energy gap (E.G.) of the tube changes with the change in its chirality and diameter.[11,12] The transport mechanism is directly reliant on the intrinsic charge carrier concentration (n-CNT) of the nanotube, written as Eq. 3.

$$n_{\mathrm{CNT}} = \int_{E_c}^{\infty} D(E)f(E)\mathrm{d}E \tag{3}$$

Let V_{SS} and V_{DS} be the source-to-substrate and drain-to-substrate voltages, respectively, then the drain current $\mathrm{I_{DS}}$ can be calculated using the Launder equation as[13]:

$$I_{\mathrm{DS}} = \frac{qkT}{\pi h}\left\{\ln\left[1+e\frac{\Delta E_F + q(\Psi_{\mathrm{cnt}}(0) - V_{\mathrm{SS}} - \Phi_0) - E_C}{KT}\right] - \ln\left[1+e\frac{\Delta E_F + q(\Psi_{\mathrm{cnt}}(L) - V_{\mathrm{DS}} - \Phi_0) - E_C}{KT}\right]\right\} \tag{4}$$

where q is the electronic charge and h is Plank's constant. Ψ_{cnt} and Φ_0 are the CNT surface potential owing to the front gate and back gate (substrate), respectively. For the top gate device structure, Φ_0 is fixed to zero. The value of Ψ_{cnt} is altered at the source and drains, which can be 0.15.

$$\Psi_{\mathrm{cnt}}(0) = V_{\mathrm{GS}} - V_{\mathrm{fb}} \tag{5}$$

where V_{fb} is flat band voltage.

Figure 2b shows the conventional type CNTFET. Because of its identical structure to the conventional MOSFET, it is called the conventional CNTFET.[14] The source and drain are densely doped and the un-gated region consists of intrinsic CNTFET; therefore, it depicts both conventional P-type and N-type CNTFET. The value of on-drain current can be induced through the channel through the quantity of charge and not by the doping concentration in the source region. The off-drain current is limited due to the absence of SB by hot radiation rather than that of direct tunneling, which concludes within feasible values of subthreshold swing. Figure 2c shows the T-CNTFET; if we introduce the p–i–n or n–i–p doping profiles alongside the CNT channel instead of n–i–n or p–i–p, the outcome is T-CNTFET structure. The device is so named as it is based on the tunneling behavior of the CNTFET. Figure 2d shows a partially gated P-type CNTFET in which the channel is intrinsic or uniformly doped (p or n). These devices work in depletion mode as there is uniform doping through

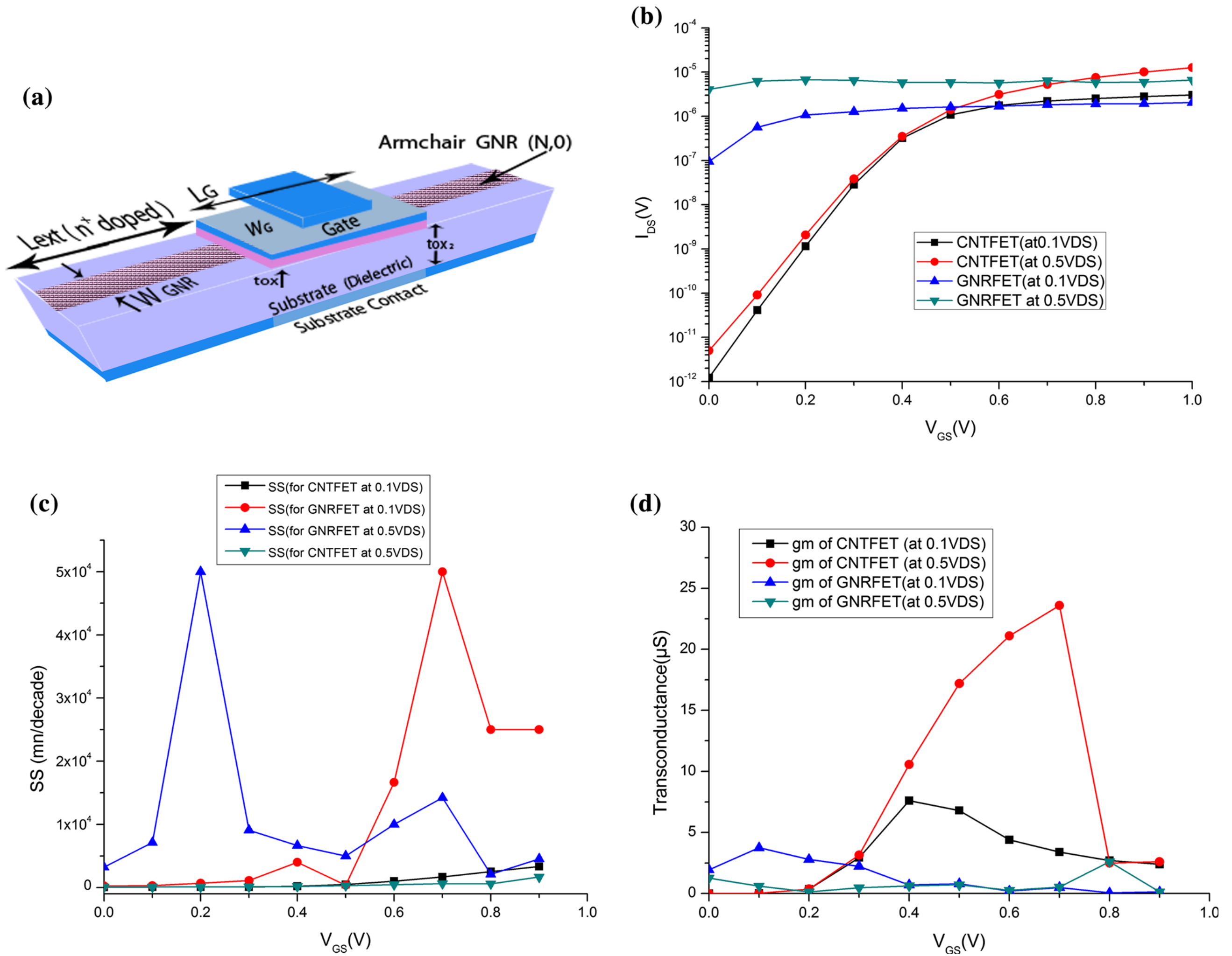

Fig. 3. (a) 3-D view of GNRFET (graphene nanoribbon field effect transistor). (b) $I_{DS} - V_{GS}$ Characteristics for CNTFET and GNRFET. (c) Subthreshold Swing (SS) comparison for CNTFET and GNRFET. (d) G_m comparison for CNTFET and GNRFET.

the channel. This device expresses p-type or n-type behavior depending on the type of doping. The CNTFET designed has CNT diameter = 1 nm, channel length = 45 nm (Ls = Ld = Lg = 15 nm), and oxide thickness = 1 nm. By considering these parameters $I_{DS} - V_{GS}$ characteristics are analyzed at constant V_{DS} as shown in Fig. 3b.

GNRFET DEVICE STRUCTURE

The valence band and conduction bands coincide in the GNR at the K points of the Brillouin zone and are cone-shaped. Because zero band gap devices with channels made of large-area graphene cannot perform switching actions, they are not suitable for circuit applications.[6,15] GNR structures are sandwiched between two insulator layers. The designed GNRFET is an armchair GNR with $N = 6$, the gate and channel lengths are equal to 15 nm, oxide thickness (t_{ox}) is 1 nm for top and bottom gate thicknesses, SiO_2 intrinsic GNR is 10 nm, length of the source and drain region is 10 nm and width of the SiO_2 layer is 0.87 nm. The thickness of the SiO_2 gate insulator is 1 nm along with a relative dielectric constant (K) value 3.9.[16] The source (drain) region of the GNR is doped at 5×10^{-3} dopants/atom. It has been analyzed that if there is an increase in bandwidth, then the width of the nanoribbon is reduced, i.e. they are inversely proportional to each other for both the armchair and zigzag nanoribbon.[17]

Analog applications are treated as increasing without barrier due to the zero band gap. Graphene-based FETs address graphene's outermost important properties, higher mobility and large saturation velocity.[18] because of the absence of band gap in graphene, analog applications are affected adversely. As drift velocity saturation does not exist in short-channel devices and inter-band tunneling suppresses current saturation, the intrinsic voltage gain is calculated as $Av_0 = g_m/g_0$, where g_0 represents output conductance.[19] Figure 3a represents

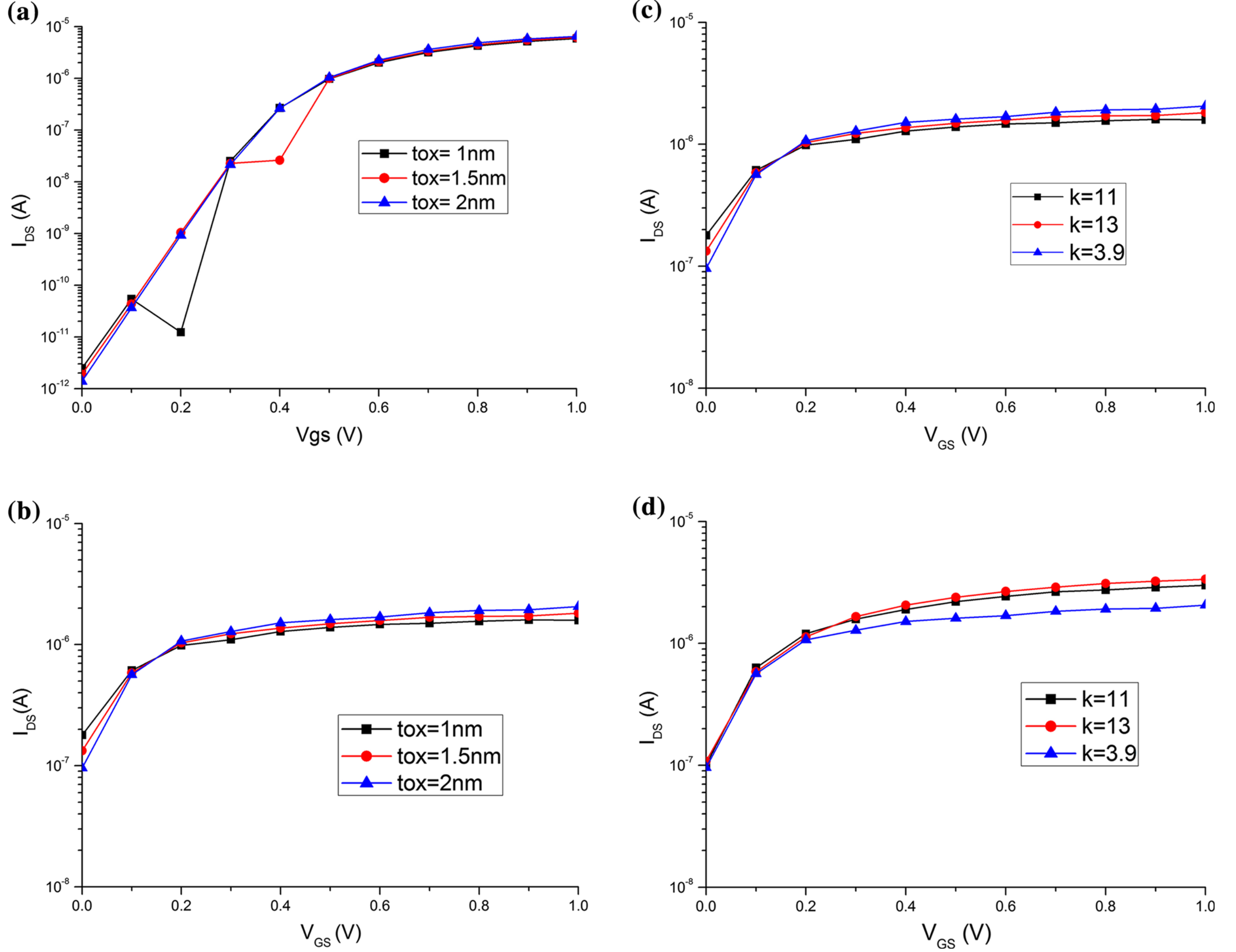

Fig. 4. (a) Effect of changing tox on I–V characteristics of CNTFET at constant V_{Ds} = 0.1 V. (b) Effect of changing tox on I–V characteristics of GNRFET at constant V_{Ds} = 0.1 V. (c) Effect of changing K on I–V characteristics CNTFET at constant V_{Ds} = 0.1 V. (d) Effect of changing K on I–V characteristics GNRFET at constant V_{Ds} = 0.1 V.

the 3-D view of a GNRFET. This structure is demonstrates a higher I_{ON}/I_{OFF} ratio, surpassing the GNRFET with Schottky barriers in logic applications. For factual clarification of electrostatic in short-channel transistors, an advantageous approach is a 3-D simulation. For this functionality, we have created a code for the simulation of GNRFETs based on the non-equilibrium Green's function formalism (NEGF), which has been licensed in 3-D device simulator NanoTCAD ViDES.[20,21] The intrinsic GNR channel has equal length underneath as the gate contact (L_G), while its width (W_G) can be varied equally from any side of the GNR channel. The width of the intrinsic GNR is calculated as below:

$$W_{GNR} = (N+1)\sqrt{3}a_{cc}/2 \tag{6}$$

where a_{cc} is the carbon–carbon bonding distance (0.144) and N is the number of dimer lines for the armchair GNR.[22]

RESULTS AND DISCUSSION

Simulation of I-V Characteristics for CNTFET and GNRFET

CNT is used for low power applications because it has a very low value of I_{OFF}. The replicas are performed for CNTFET by taking CNT = 13, d = 1 nm, tox = 1 nm, L_C = 15 nm and similarly for GNRFET by taking N = 6, tox = 1 nm and L_C = 15 nm. Simulations are performed by making V_{DS} constant as 0.1 V, 0.5 V and varying V_{GS} from 0 V to 1 V for subthreshold leakage current. The outcomes are correlated with the simulation waveform of GNRFET, and hence it is concluded that GNRFET gives ultra-high subthreshold swing in comparison with CNTFET for same parameters as shown in Fig. 3c.

I_{ON}/I_{OFF} Calculation

The simulations for $I_D - V_{GS}$ are also compared in order to interpret the I_{ON} and I_{OFF} and, therefore,

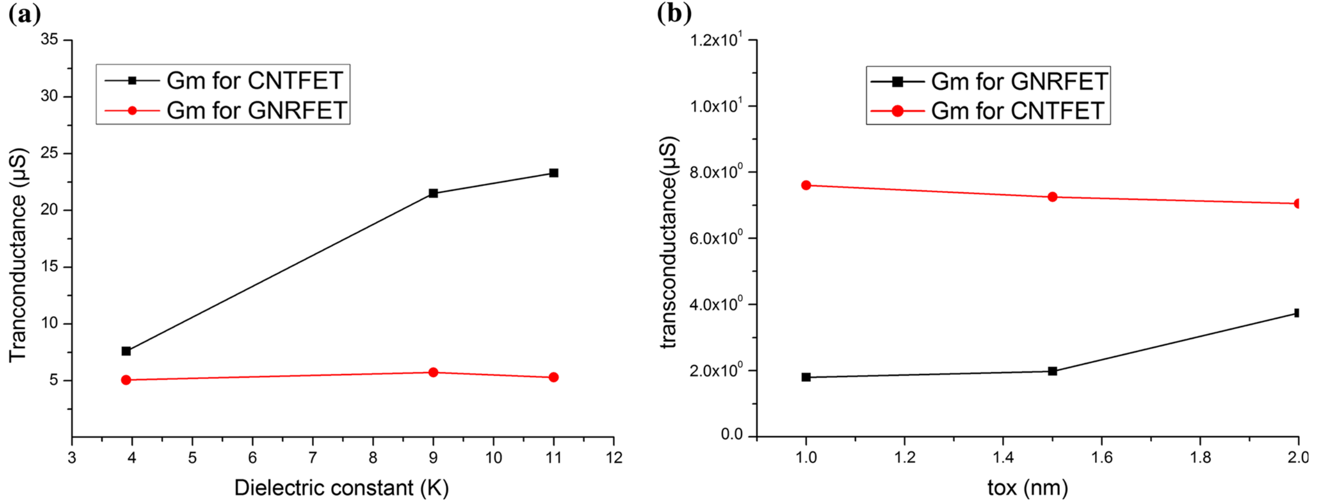

Fig. 5. (a) G_m versus K for CNTFET and GNRFET. (b) G_m versus tox for CNTFET and GNRFET.

I_{ON}/I_{OFF} ratio. CNTFET offers very low I_{OFF} current of the order of 10^{-12} and GNRFET offers the order of 10^{-06} , which makes CNTFET more convenient for low power applications. But CNTFET offer little higher I_{ON} current of the order of 10^{-06} in comparison to GNRFET with 10^{-05}, which makes them good enough for high performance. The calculated I_{ON}/I_{OFF} ratio is on the order of 10^{06} and 10^{01} for CNTFET and GNRFET, respectively. The current ratio I_{ON}/I_{OFF} is high in CNTFET than GNRFET, which shows that CNTFET is more useful for low power applications. The reason for the decrease in I_{ON} current due to the increase in the roughness amplitude is because of the increase in carrier scattering associated with line edge roughness. The critical roughness amplitude corresponds to the maximum I_{OFF} and minimum I_{ON} current. In GNR very high I_{OFF} associated with the small band gap and GNR band gap decreases for larger nanoribbons. Figure 3b show the $I_{DS} - V_{GS}$ characteristics for CNTFET and GNRFET.

Table I. Performance comparison of parameters at V_{DS} = 0.1 V

Parameters calculated	CNTFET	GNRFET
I_{ON} (A)	3.05E−06	1.428E−06
I_{OFF} (A)	1.22E−12	1.185E−07
(I_{ON}/I_{OFF})	2.52E+06	1.25E−01
SS (mV/dec)	64.4	236
G_m (μS)	7.6	3.74

Table II. Performance comparison of parameters at V_{DS} = 0.5 V

Parameters calculated	CNTFET	GNRFET
$I_{ON}(A)$	1.27E−05	2.61E−06
$I_{OFF}(A)$	5.01E−12	1.72E−06
(I_{ON}/I_{OFF})	2.53E+07	1.15E−00
SS(mV/decade)	74	2083
G_m (μS)	23.6	1.26

Calculation of SS (Subthreshold Swing)

There is an important parameter or factor in digital circuits known as “subthreshold swing” (SS), defined as “how often the transistor switches to ON with the variation of the gate voltage, and vice versa”. SS should be as small as possible for more abrupt transitions. Subthreshold swing is inversely proportional to the subthreshold slope. In CNTFET, steep subthreshold slope is observed, which means small subthreshold swing. Steep subthreshold slope means that there is a faster transition between on and off current states. Figure 3c shows the SS graph for both CNTFET and GNRFET. SS value can be calculated by using the formula below[23]:

$$SS = \frac{\partial V_{GS}}{\partial(\log_{10}(I_{DS}))} \quad (7)$$

The SS values are plotted at different V_{GS} with V_{DS} = 0.1 V and 0.5 V for both CNTFET and GNRFET as shown in Fig. 3c. CNTFET offers a minimum SS value of 64.4 mV/dec, whereas GNRFET offers a value of 236 mV/dec at V_{DS} = 0.1 V. It is also observed that CNTFET offers a value of 74 mV/de, whereas GNRFET offers 2083 mV/dec corresponding to V_{DS} = 0.5 V. From this, it can be observed that CNTFET offers a minimum value of SS as compared to GNRFET, which means better channel control, hence improved I_{ON}/I_{OFF} ratio. Improved I_{ON}/I_{OFF} ratio means less leakage, hence less power dissipation. For this reason it is more suitable for low power digital circuits.

Table III. Effect of oxide thickness on I_{ON}/I_{OFF} and G_m at V_{DS} = 0.1 V

Oxide thickness (tox) (nm)	I_{ON}/I_{OFF} in CNTFET	I_{ON}/I_{OFF} in GNRFET	g_m for CNTFET (μS)	g_m for GNRFET (μS)
1	4.6e+06	0.16e+01	7.6	1.8
1.5	3.21e+06	0.31e+01	7.25	1.98
2	2.35e+06	0.21e+02	7.05	3.74

Table IV. Effect of Dielectric constant on I_{ON}/I_{OFF} and G_m at V_{DS} = 0.1 V

Dielectric constant (K)	I_{ON}/I_{OFF} in CNTFET	I_{ON}/I_{OFF} in GNRFET	g_m for CNTFET (μS)	g_m for GNRFET (μS)
3.9(SiO_2)	4.6e+06	0.16e+01	7.6	5.06
9(Al_2O_3)	6.3e+06	2.97e+01	21.5	5.73
11(HfO_2)	6.7e+06	3.11e+01	23.3	5.45

Calculation of Trans-conductance

Trans-conductance (g_m) is also another important parameter, which decides the analog device sensitivity for sensor application. When channel length scales down to 10 nm, trans-conductance decreases because the gate has worse control over the channel due to electrostatic short channel devices. Trans-conductance (g_m) can be computed by using the formula below:

$$g_m = \frac{\partial I_{DS}}{\partial V_{GS}} \quad (8)$$

Figure 3d shows g_m values, computed for varying V_{GS} from 0 V to 1 V. The maximum value of g_m as calculated 3.74 μS for GNRFET, whereas for CNTFET it is 7.6 μS at V_{GS} = 0.1 V (Table I). At V_{GS} = 0.5 V the value of gm is 1.26 μS for GNRFET and 23.6 μS for CNTFET (Table II). After comparing these values and from Fig. 3d, it is observed that the value of trans-conductance is higher for CNTFET, which makes it a good substitute in analog circuits.

Effect of Oxide Thickness and Dielectric Constant on CNTFET and GNRFET

Figure 4a and b shows the effect of oxide thickness on CNTFET and GNRFET at constant V_{DS} = 0.1 V and for the same channel length of 15 nm. From this we analyzed that the I_{ON}/I_{OFF} current ratio decreases with increase in oxide thickness, which means that I_{ON}/I_{OFF} ratio is inversely proportional to the oxide thickness in CNTFET, whereas in the case of GNRFET, they are directly proportional to each other. Figure 4c and d shows the effect of dielectric constant on I–V characteristics of CNTFET and GNRFET at the same channel length and V_{DS} = 0.1 V. Figure 5a and b shows that trans-conductance decreases with an increase in oxide thickness in CNTFET, but in GNRFET they are inversely proportional to each other (Table III). Trans-conductance increases with the increase in dielectric constant both in the case of GNRFET and CNTFET. This means that K is directly proportional to G_m (Table IV). Lastly, the graphs between G_m versus K and G_m versus T_{ox} are plotted as shown below.

CONCLUSION

This paper presents a comparative analysis of CNTFET and GNRFET based on various performance specifications, which are listed as I_{ON}/I_{OFF} current ratio, trans-conductance and inverse sub-threshold slope. Extensive NanoTCAD VIDES simulations have been performed to compute the performance parameters. It is concluded from the results obtained that CNTFET offers better performance including I_{ON}/I_{OFF} ratio, steep inverse sub-threshold swing (SS), and trans-conductance than GNRFET. Effect of oxide thickness and dielectric constant is also studied for CNTFET and GNRFET for the same channel length and at constant V_{DS} voltage. Hence, CNTFET performs much better for the future scope for nanoscale devices as compared to GNRFET. For future works, the temperature and chirality responses can be observed on the performance of CNTFET and GNRFET.

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